Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended). A power transistor having at least one trench transistor cell in a semiconductor body, comprising:

a drain zone, a drift zone, a channel zone, and a source zone formed in each case successively and substantially horizontally in the semiconductor body;

the semiconductor body having a trench formed therein with a base and a defined body height opposite a pn junction between said drift zone and said channel zone;

a first dielectric layer cladding said trench substantially to said body height, and a gate oxide cladding said trench between said body zone and a semiconductor body surface; and

a field electrode extending in said trench substantially from said trench base to an upper edge of said first dielectric layer, said field electrode being connected to be at a fixed potential or at a source potential;

a gate electrode disposed substantially between said body height and the semiconductor body surface, said gate electrode being electrically insulated from the semiconductor body by said gate oxide and having a lower edge with a profile at least partly different from horizontal; and

a second dielectric layer formed between said gate electrode and said field electrode.

Claim 2 (original). The power transistor according to claim 1, wherein said profile of said lower edge of said gate electrode is at least partly angled relative to the semiconductor body surface.

Claim 3 (original). The power transistor according to claim 2, wherein said profile has a falling angle between two trenches.

Claim 4 (original). The power transistor according to claim 1, wherein said profile of said lower edge of said gate electrode is formed with at least one outward bulge.

Claim 5 (original). The power transistor according to claim 1, wherein said field electrode overlaps said gate electrode.

Claim 6 (original). The power transistor according to claim 5, wherein at least one of said field electrode and said gate electrode intersects and/or passes through a plane defined by said pn junction between said drift zone and said channel zone.

Claims 7-8 (cancelled).